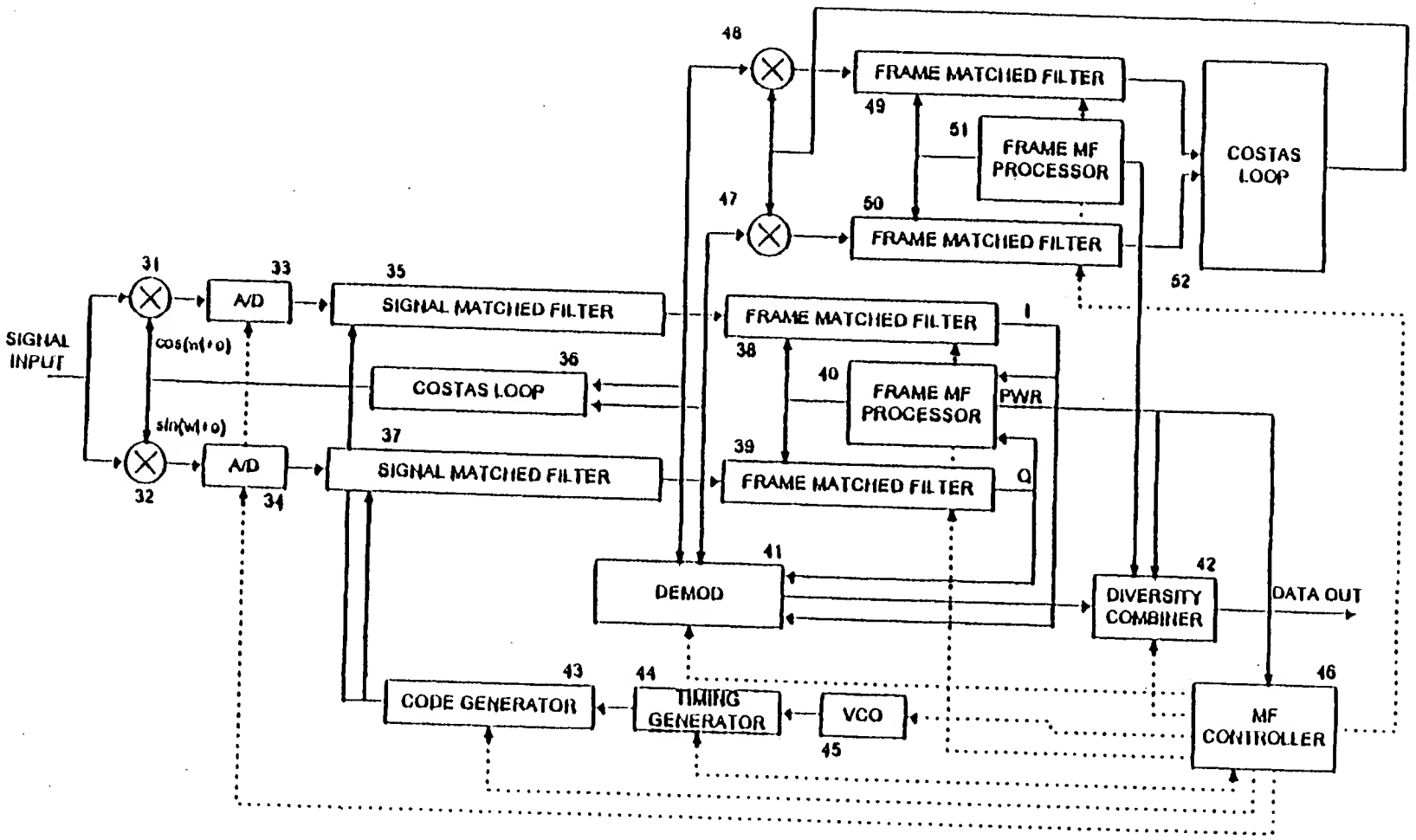

SIGNAL INPUT
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
A/D
A/D
cos(w(+o)
sin(w(+o)
SIGNAL MATCHED FILTER
SIGNAL MATCHED FILTER
COSTAS LOOP
FRAME MATCHED FILTER
FRAME MATCHED FILTER
FRAME MATCHED FILTER
FRAME MATCHED FILTER
FRAME MF PROCESSOR
FRAME MF PROCESSOR
COSTAS LOOP
I
Q
PWR
DEMOD
DIVERSITY COMBINER
DATA OUT
CODE GENERATOR
TIMING GENERATOR
VCO
MF CONTROLLER

FIGURE 1.

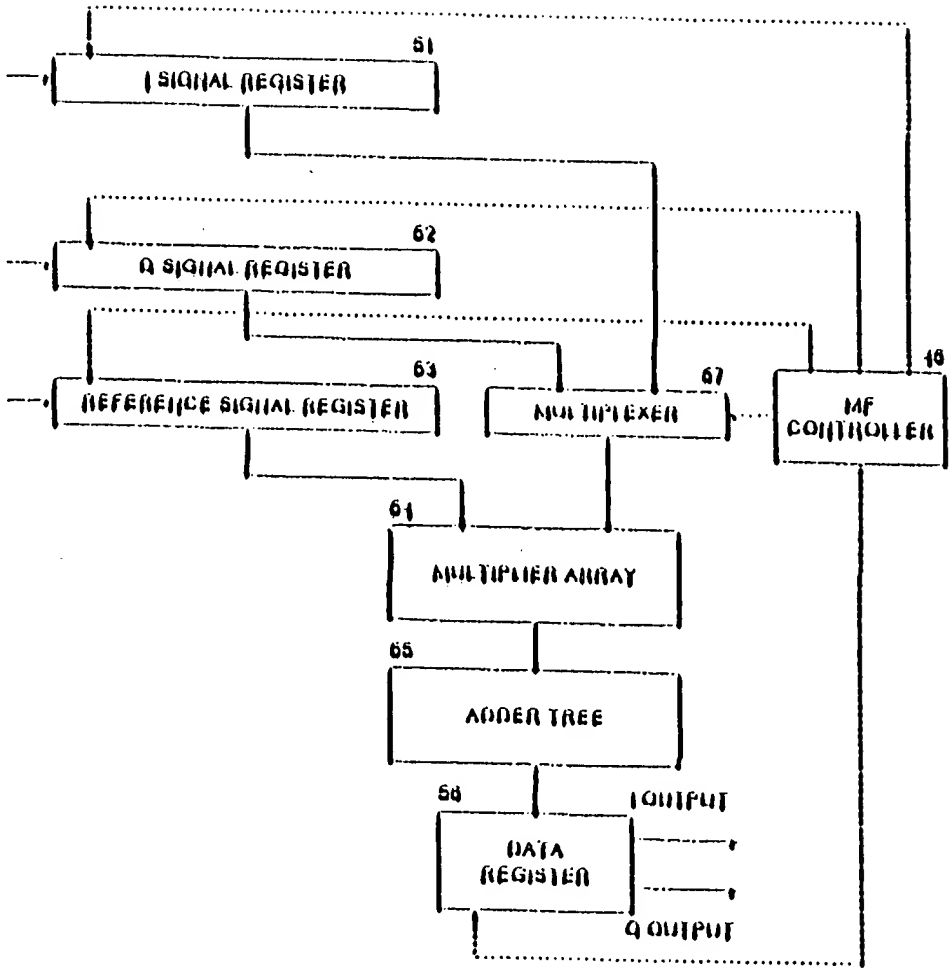

61
I SIGNAL REGISTER
62
Q SIGNAL REGISTER
63
REFERENCE SIGNAL REGISTER
67
MULTIPLEXER
MF CONTROLLER
16
64
MULTIPLIER ARRAY
65
ADDER TREE
68
I OUTPUT
DATA REGISTER
Q OUTPUT

FIGURE 2

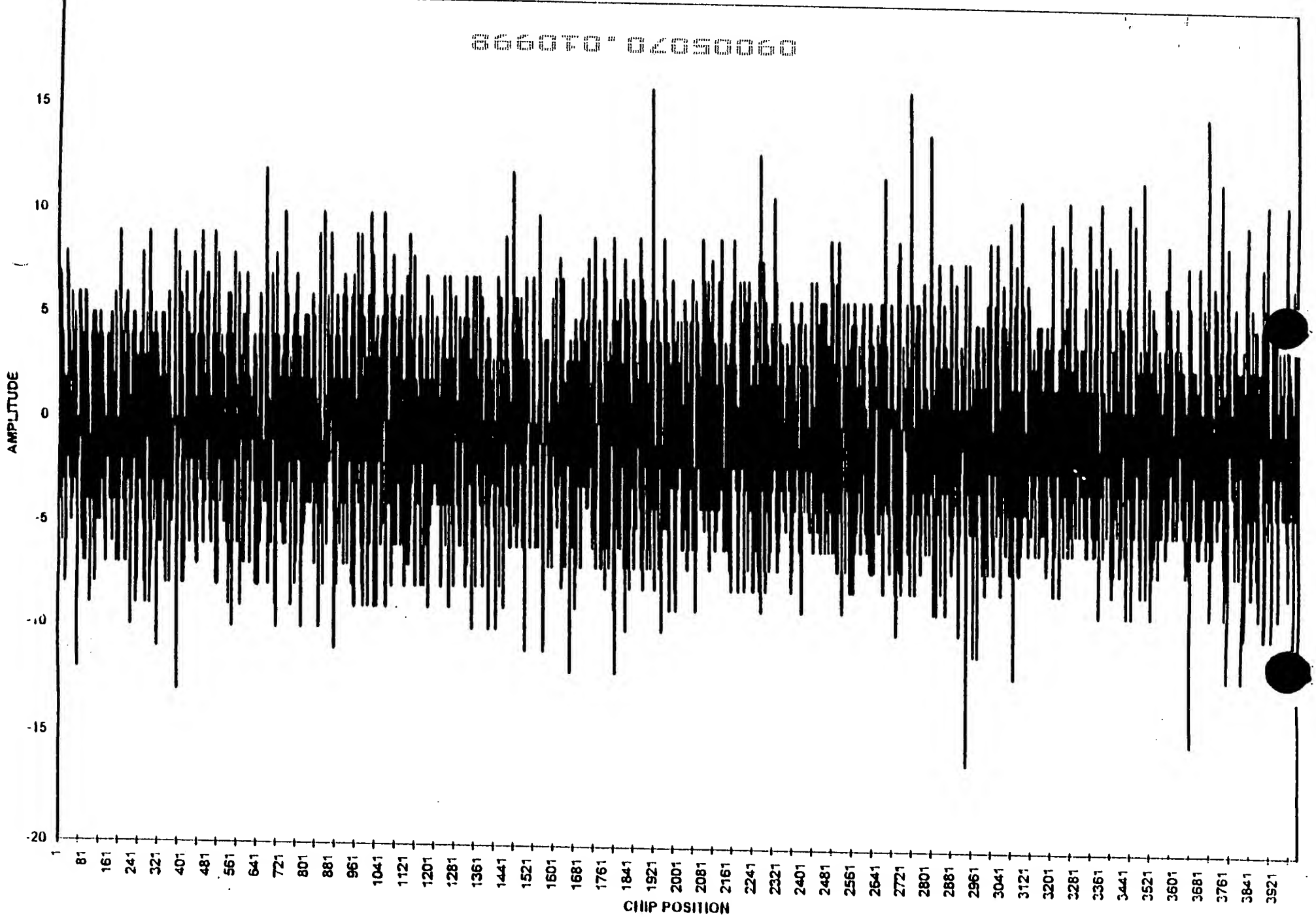

AMPLITUDE
15
10
5
0
-5
-10
-15
-20
1
81
161
241
321
401
481
561
641
721
801
881
961
1041
1121
1201
1281
1361
1441
1521
1601
1681
1761
1841
1921
2001
2081
2161
2241
2321
2401
2481
2561
2641
2721
2801
2881
2961
3041
3121
3201
2281
2361
3441
3521
3601
3681
3761
3841
3921
CHIP POSITION

FIG. 3

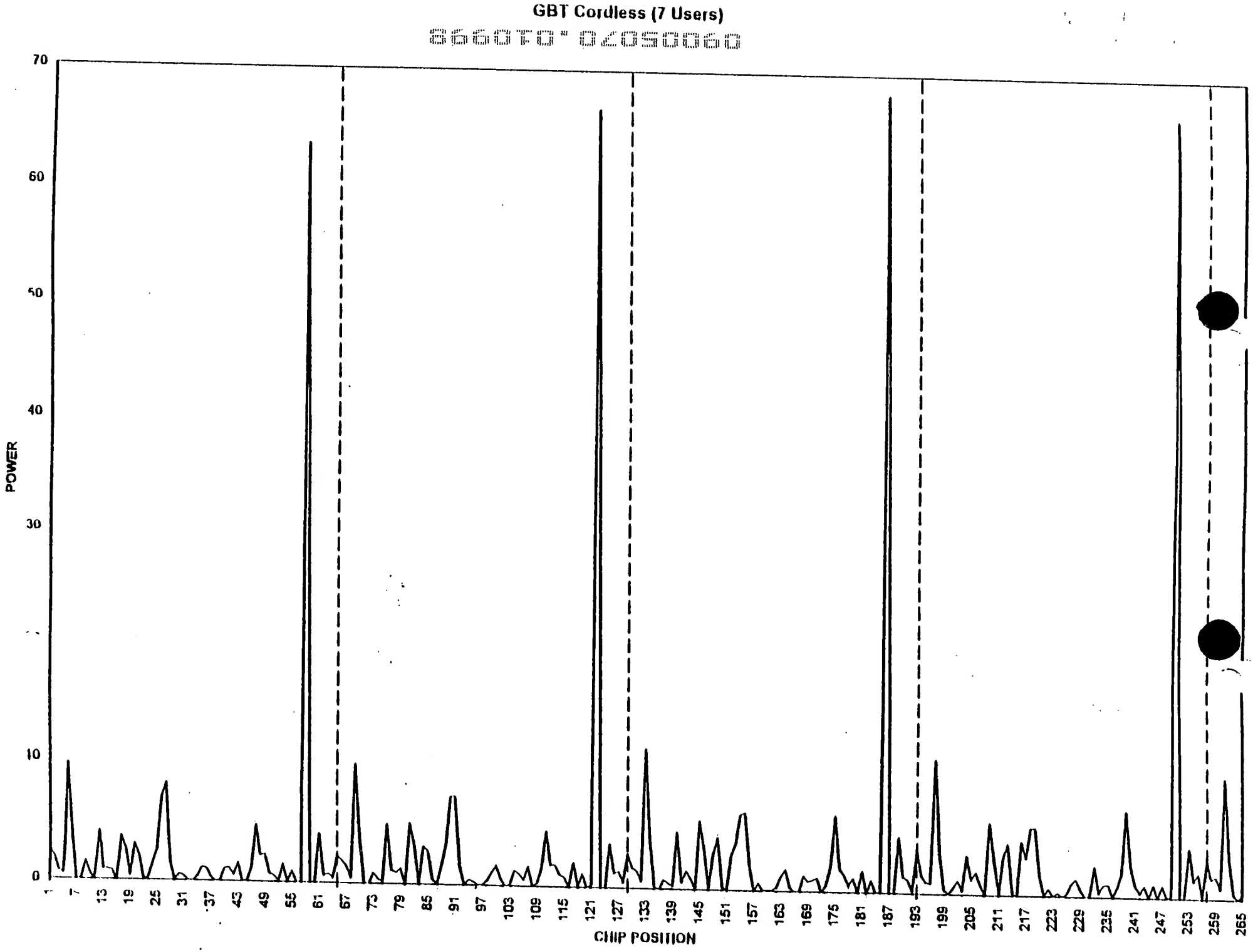

GBT Cordless (7 Users)
70
60
50
40
30
10
0
POWER
CHIP POSITION
1
7
13
19
25
31
37
43
49
55
61
67
73
79
85
91
97
103
109
115
121
127
133
139
145
151
157
163
169
175
181
187
193
199
205
211
217
223
229
235
241
247
253
259
265

FIG. 4

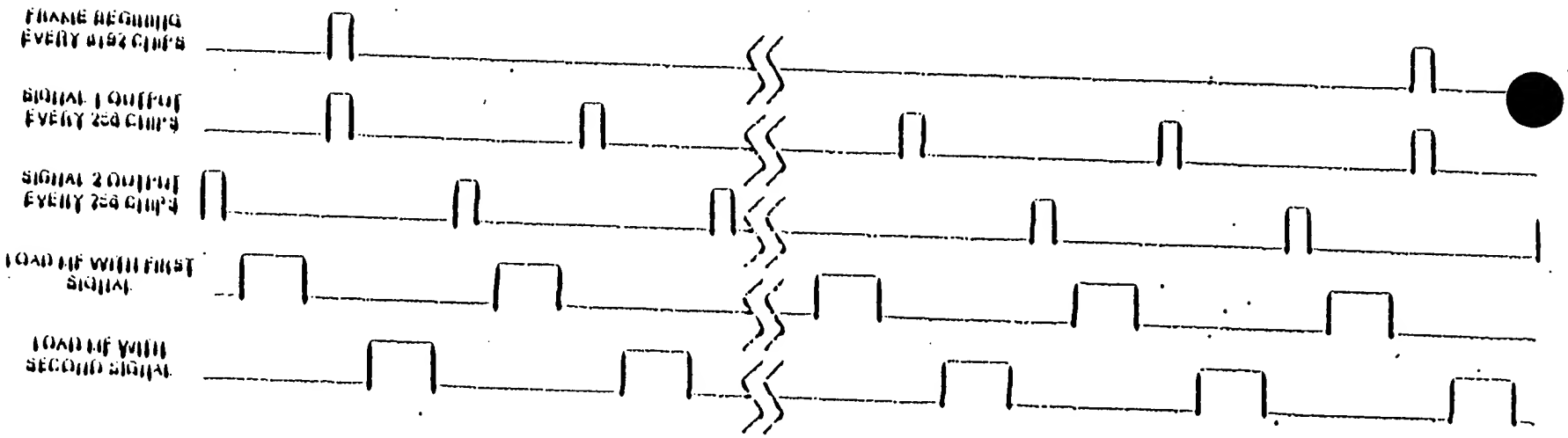

FRAME BEGINNING
EVERY 8192 CHIP'S
SIGNAL 1 OUTPUT
EVERY 256 CHIP'S
SIGNAL 2 OUTPUT
EVERY 256 CHIP'S
LOAD HF WITH FIRST
SIGNAL
LOAD HF WITH
SECOND SIGNAL

FIGURE 5

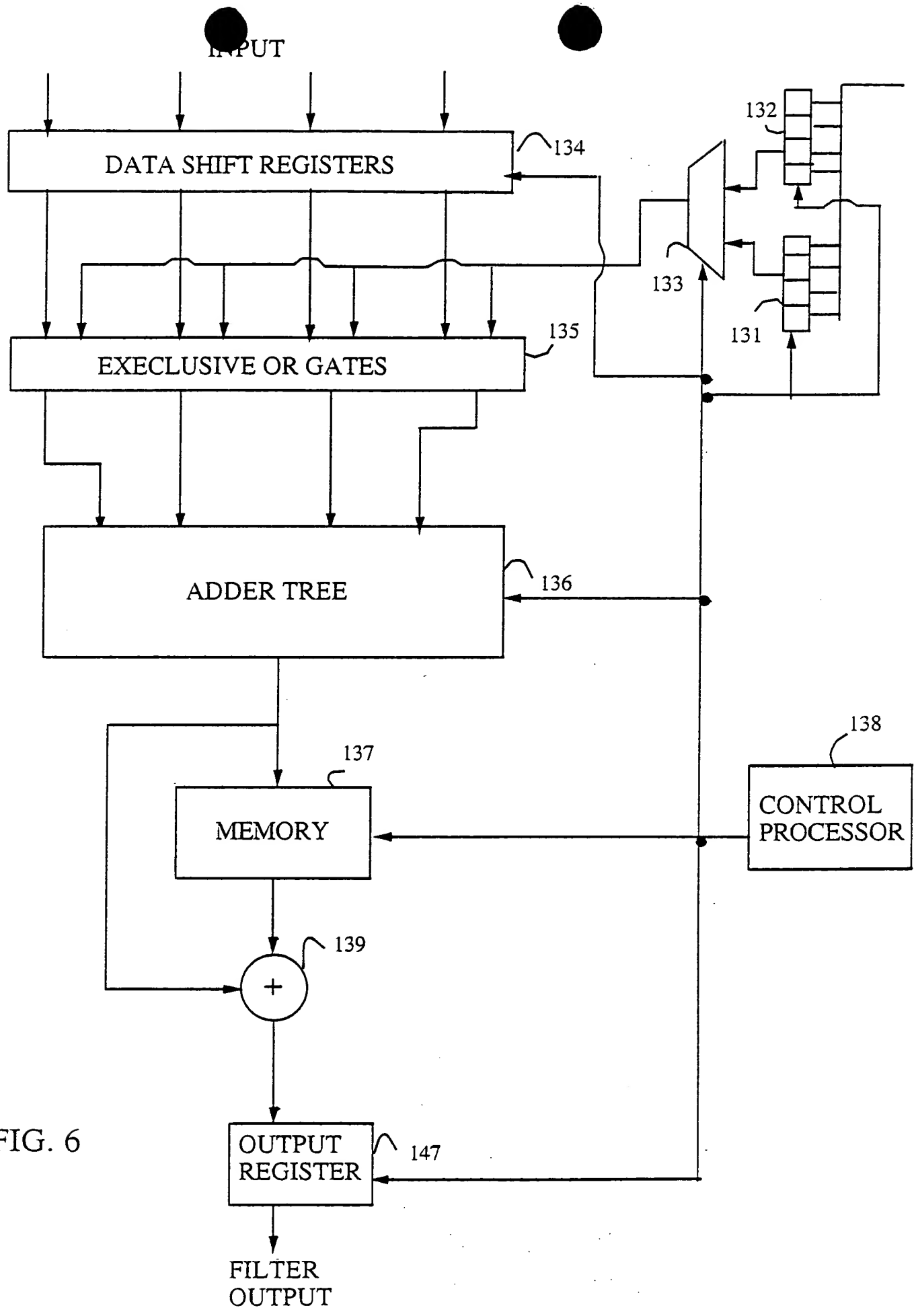

INPUT
DATA SHIFT REGISTERS
134
132
133
131
EXECLUSIVE OR GATES
135
ADDER TREE
136
138
137
MEMORY
CONTROL PROCESSOR
139
+
OUTPUT REGISTER
147
FILTER OUTPUT

FIG. 6

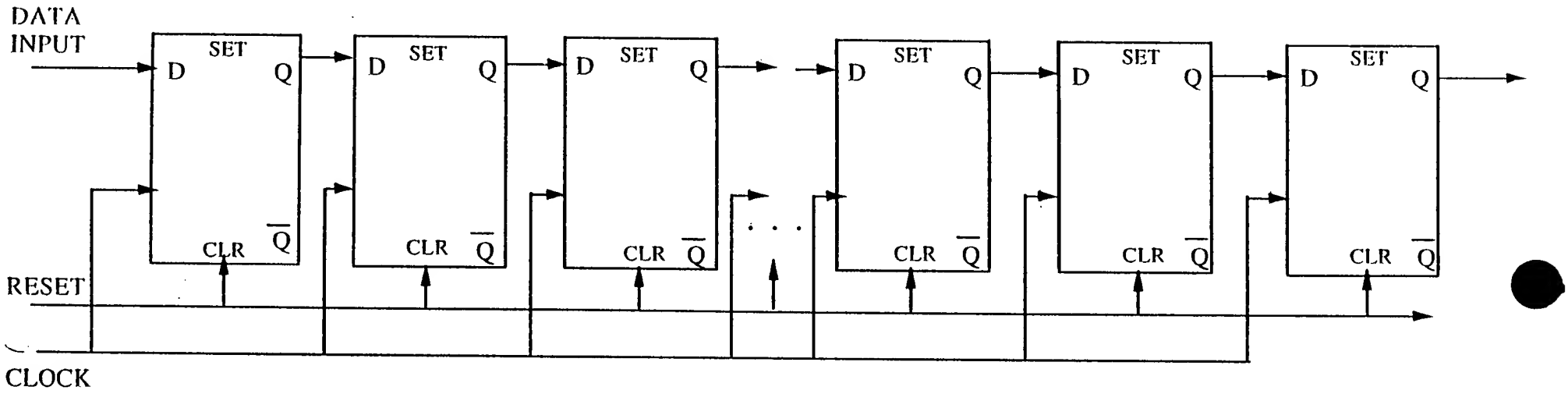

DATA
INPUT
SET
D
Q
CLR
RESET
CLOCK

FIG. 7

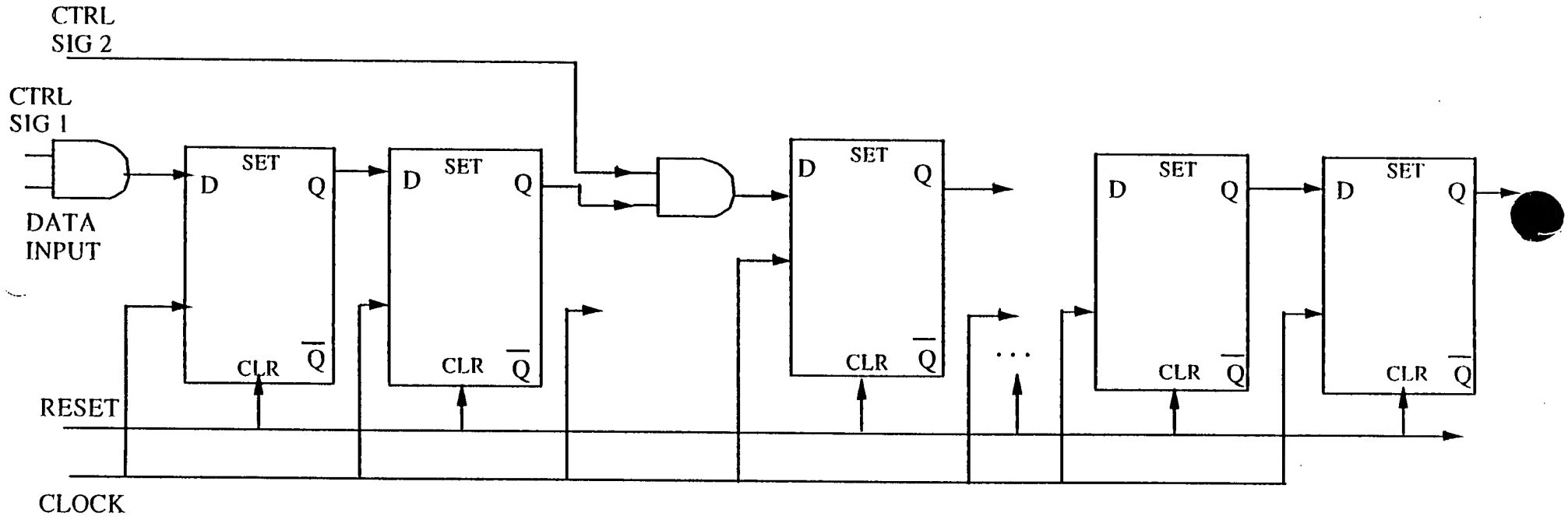

CTRL
SIG 2
CTRL
SIG 1
DATA
INPUT
SET
D
Q
CLR
RESET
CLOCK

FIG. 8

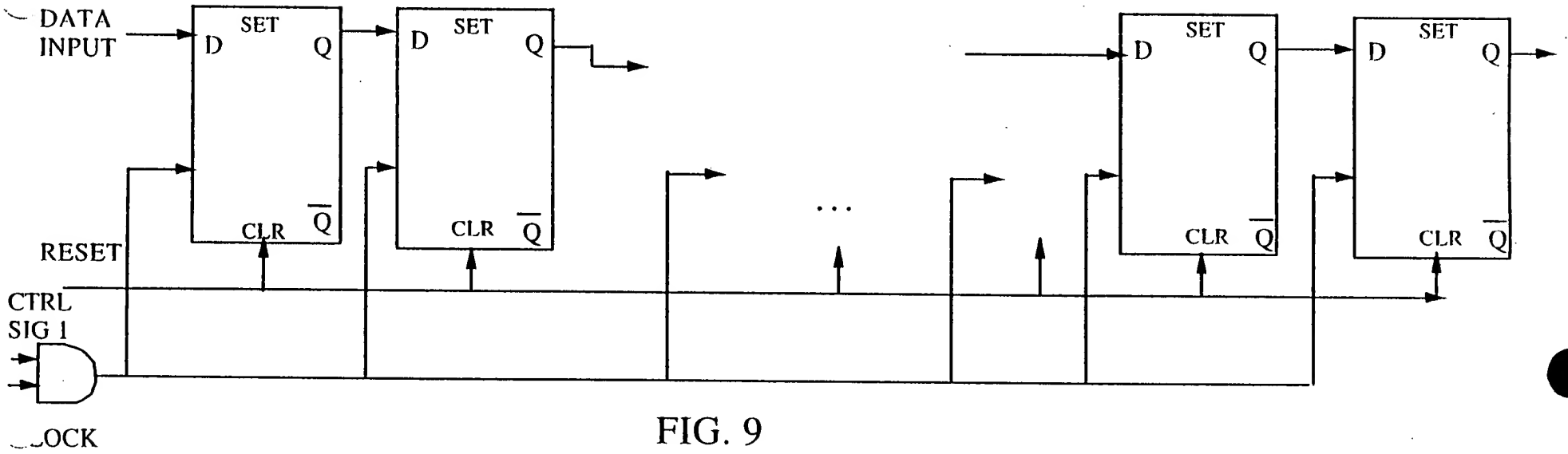


FIG. 9

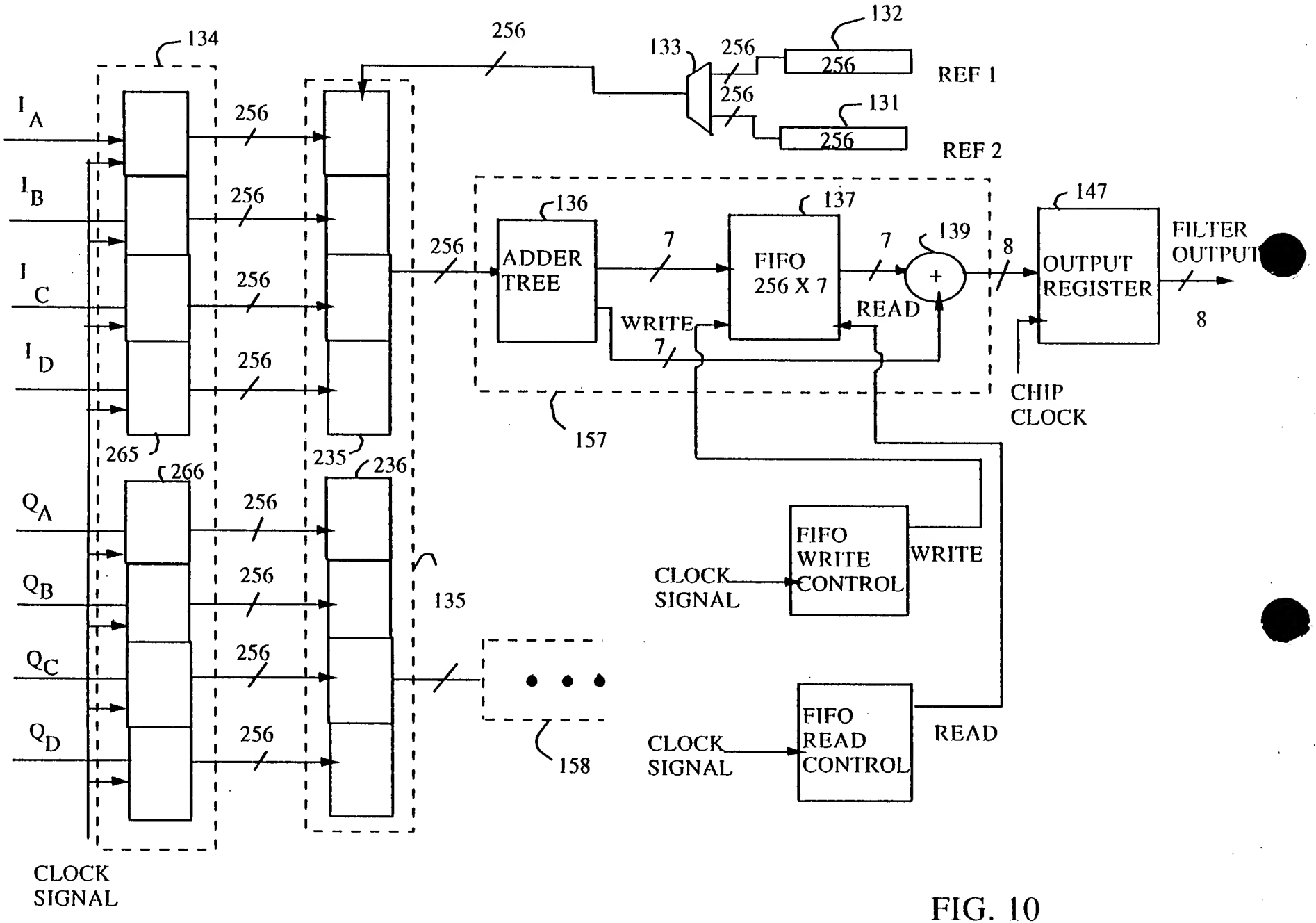

134
256
132
133
256
256
REF 1
256
131
256
REF 2
I_A
I_B
I_C
I_D
256
256
256
256
265
235
236
266
Q_A
Q_B
Q_C
Q_D
256
256
256
256
135
158
CLOCK SIGNAL
256
136
ADDER TREE
7
137
FIFO 256 X 7
7
139
+
8
147
OUTPUT REGISTER
FILTER OUTPUT
8
WRITE
7
READ
157
CHIP CLOCK
FIFO WRITE CONTROL
CLOCK SIGNAL
WRITE
FIFO READ CONTROL
CLOCK SIGNAL
READ

FIG. 10

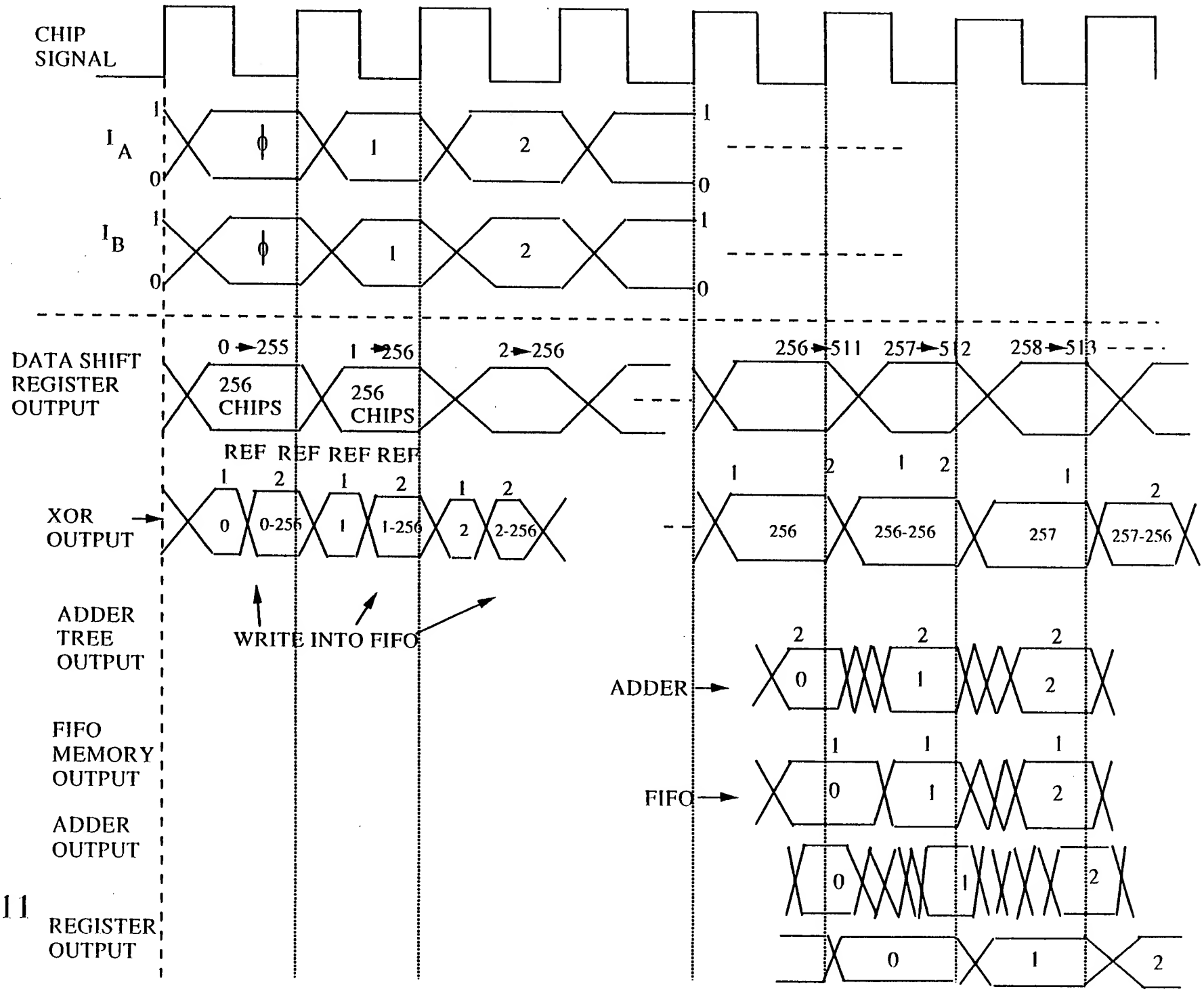
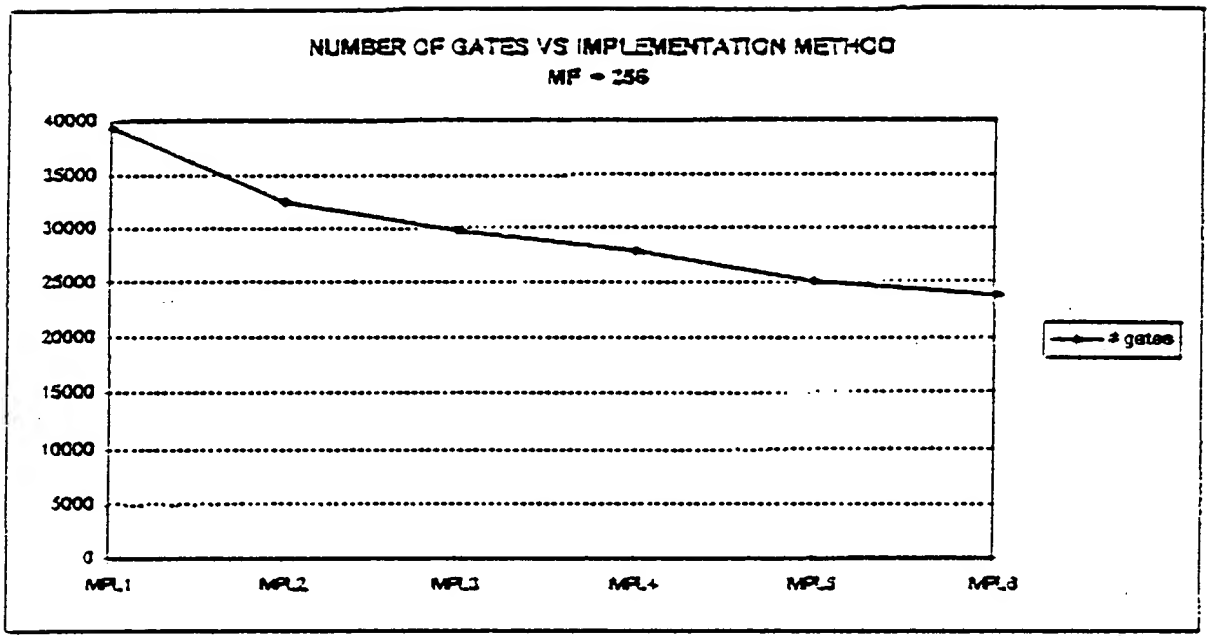

CHIP SIGNAL
I A
I B
DATA SHIFT REGISTER OUTPUT
0 ►255
1 ►256
2►256
256 CHIPS
256 CHIPS
256►511
257►512
258►513
REF REF REF REF
XOR OUTPUT
0
0-256
1
1-256
2
2-256
256
256-256
257
257-256
ADDER TREE OUTPUT
WRITE INTO FIFO
ADDER
FIFO
FIFO MEMORY OUTPUT
ADDER OUTPUT
REGISTER OUTPUT

FIG. 11

FIG. 12


NUMBER OF GATES VS IMPLEMENTATION METHOD
MF = 256
40000
35000
30000
25000
20000
15000
10000
5000
0
MPL1
MPL2
MPL3
MPL4
MPL5
MPL6
gates

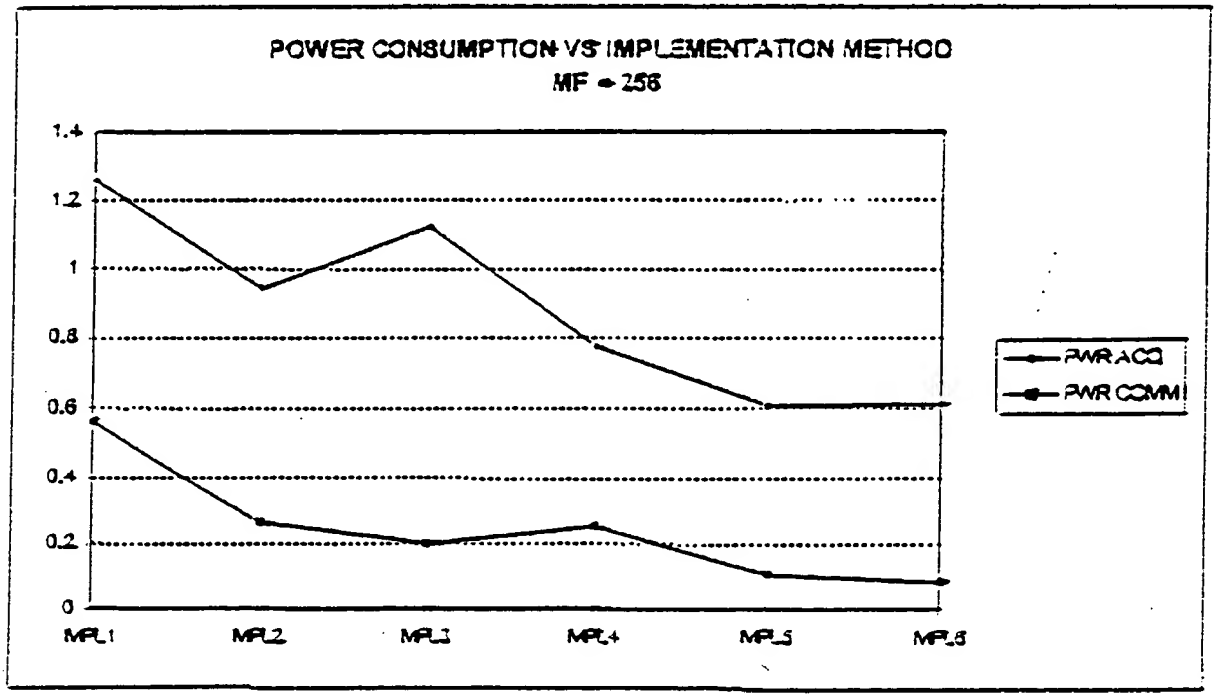
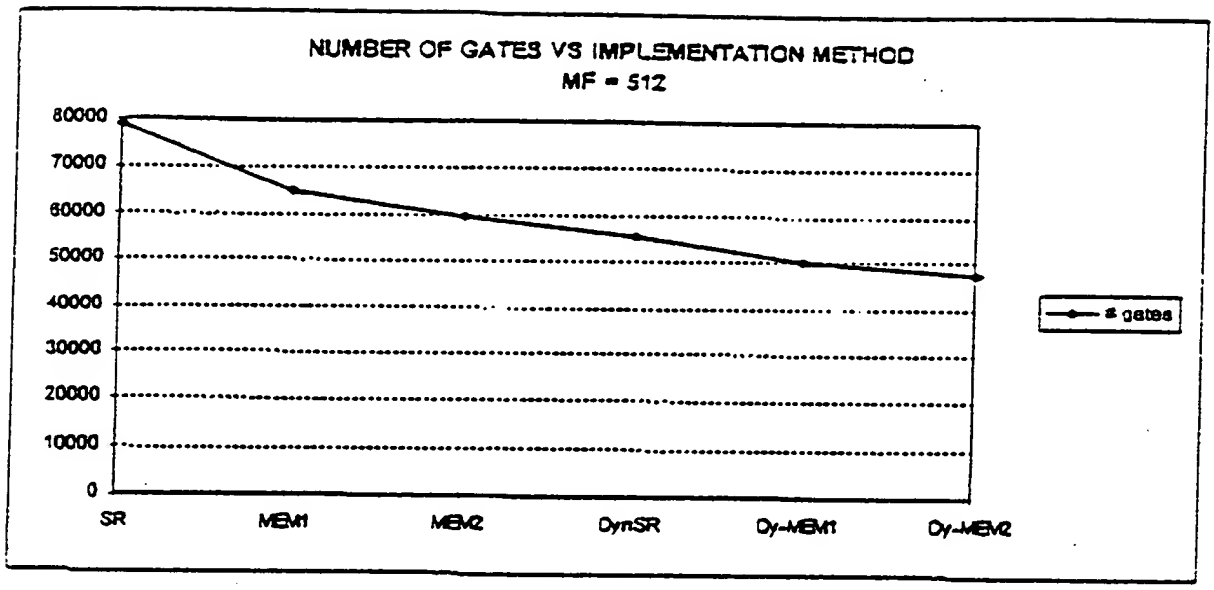

POWER CONSUMPTION VS IMPLEMENTATION METHOD
MF = 256
1.4
1.2
1
0.8
0.6
0.4
0.2
0
MPL1
MPL2
MPL3
MPL4
MPL5
MPL6
PWR ACQ
PWR COMM

FIG. 13

FIG. 14


NUMBER OF GATES VS IMPLEMENTATION METHOD
MF = 512
80000
70000
60000
50000
40000
30000
20000
10000
0
SR
MEM1
MEM2
DynSR
Dy-MEM1
Dy-MEM2
gates

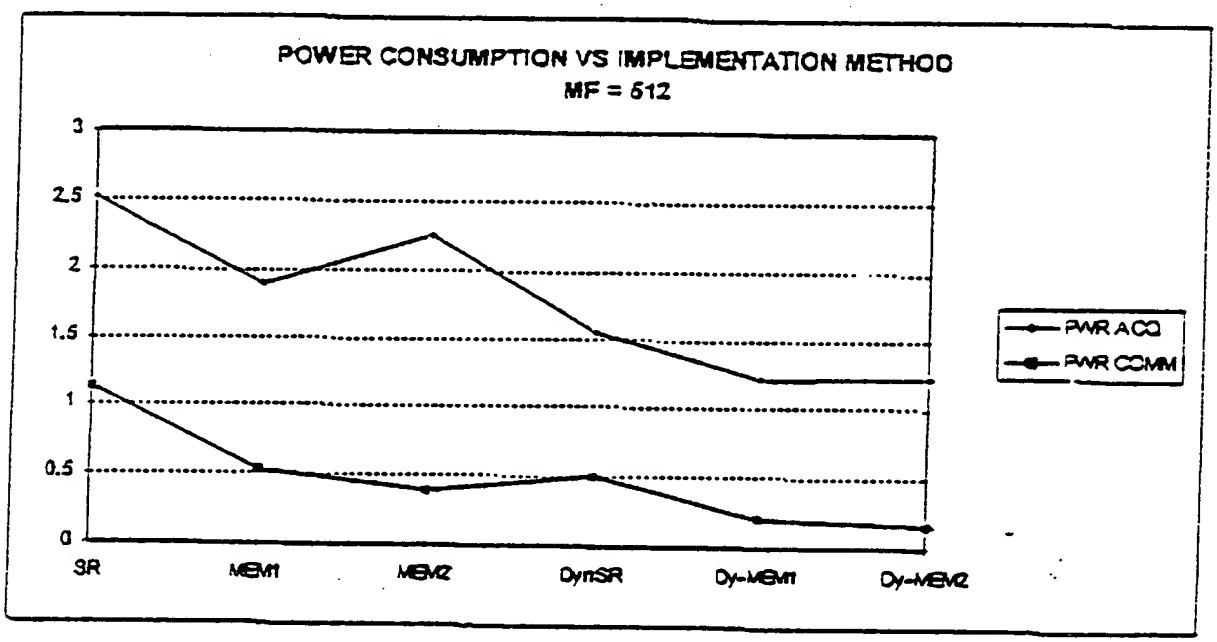

POWER CONSUMPTION VS IMPLEMENTATION METHOD
MF = 512
3
2.5
2
1.5
1
0.5
0
SR
MEM1
MEM2
DynSR
Dy-MEM1
Dy-MEM2
PWR ACQ
PWR COMM

FIG. 15

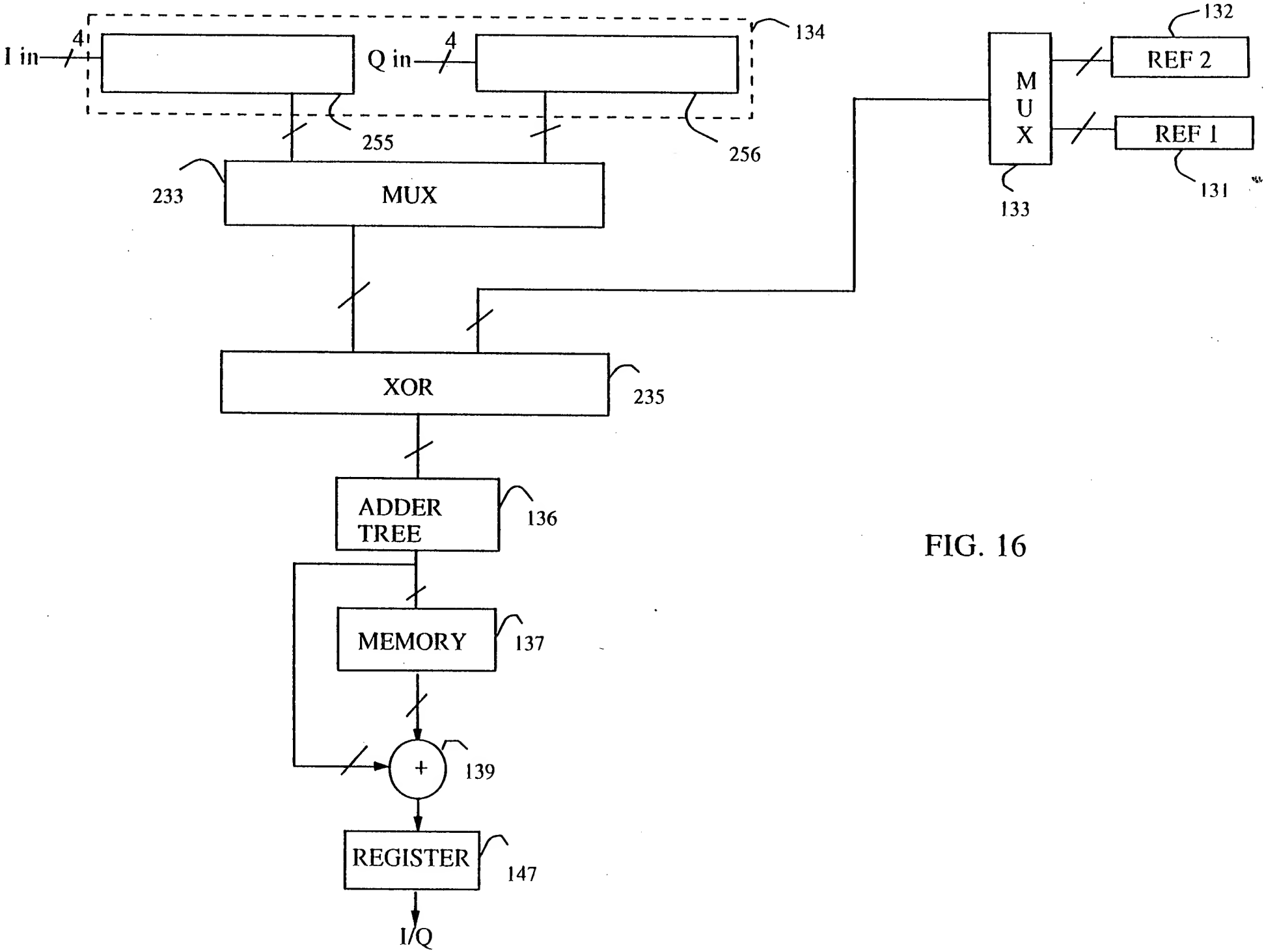

I in
4
Q in
4
134
255
256
233
MUX
132
REF 2
M
U
X
REF 1
131
133
XOR
235
ADDER
TREE
136
MEMORY
137
+
139
REGISTER
147
I/Q

FIG. 16